

PATENT ABSTRACTS OF JAPAN

(11)Publication number : 2004-198111

(43)Date of publication of application : 15.07.2004

(51)Int.Cl.

G01R 31/26
H01L 29/80

(21)Application number : 2002-363230

(71)Applicant : NIPPON TELEGR & TELEPH
CORP <NTT>

(22)Date of filing : 16.12.2002

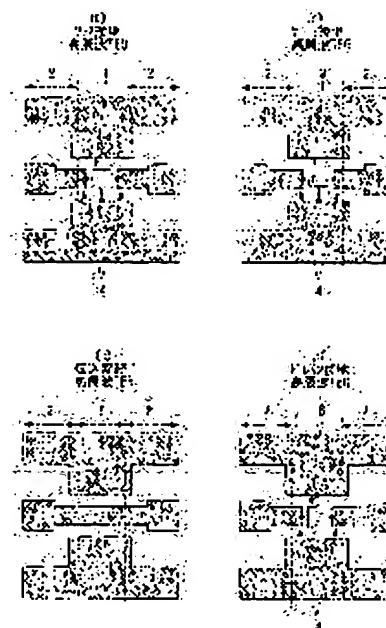
(72)Inventor : KOSUGI TOSHIHIKO
SHIBATA YUKIMICHI

(54) METHOD FOR EXTRACTING DEVICE PARAMETER OF FIELD EFFECT TRANSISTOR

(57)Abstract:

PROBLEM TO BE SOLVED: To highly precisely extract drain-source capacitance (Cds), which has been low in sensitivity to an optimum evaluation function and has not been extracted with high accuracy.

SOLUTION: In this method for extracting device parameters of a field effect transistor, both a source-grounded transistor small signal equivalent circuit and a gate-grounded transistor small signal equivalent circuit each for measuring source-grounded 2 port s-parameters of the field effect transistor and its gate-grounded 2 port s-parameters are constituted through the use of common device parameters. The fitting to the source-grounded 2 port s-parameters by the source-grounded transistor small signal equivalent circuit and the fitting to the gate-grounded 2 port s-parameters by the gate-grounded transistor small signal equivalent circuit are simultaneously performed through the use of one optimum evaluation function. The device parameters when the optimum evaluation function displays an optimum state.



LEGAL STATUS

[Date of request for examination] 27.12.2004

[Date of sending the examiner's decision of rejection]

[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]

[Date of final disposal for application]

[Patent number]

[Date of registration]

[Number of appeal against examiner's decision of rejection]

[Date of requesting appeal against examiner's decision of rejection]

[Date of extinction of right]

Copyright (C); 1998,2003 Japan Patent Office

* NOTICES *

JPO and NCIPi are not responsible for any damages caused by the use of this translation.

- 1.This document has been translated by computer. So the translation may not reflect the original precisely.
- 2.**** shows the word which can not be translated.
- 3.In the drawings, any words are not translated.

CLAIMS

[Claim(s)]

[Claim 1]

The gate electrode of the field-effect transistor by which the grounded source was carried out is made into a port 1, and a grounded source 2 port s parameter is measured by making a drain electrode into a port 2,

Although the grounded gate of this field-effect transistor was carried out, a source electrode is made into a port 1 and a grounded gate 2 port s parameter is measured by making a drain electrode into a port 2,

A grounded source transistor small signal equivalent circuit and a grounded gate transistor small signal equivalent circuit are constituted using a common device parameter,

Fitting by said grounded source transistor small signal equivalent circuit to said grounded source 2 port s parameter and fitting by said grounded gate transistor small signal equivalent circuit to said grounded gate 2 port s parameter are performed to coincidence using one optimization performance index,

The device parameter extraction method of the field-effect transistor characterized by making a device parameter when this optimization performance index shows an optimum state into an optimum solution.

[Claim 2]

In a device parameter extraction method according to claim 1,

The gate electrode of the field-effect transistor by which the grounded drain was carried out is made into a port 1, and a grounded drain 2 port s parameter is measured by making a source electrode into a port 2,

A grounded drain transistor small signal equivalent circuit is constituted using the aforementioned common device parameter,

Three persons of fitting by said grounded drain transistor small signal equivalent circuit to said grounded drain 2 port s parameter and two persons' above mentioned fitting are performed to coincidence using one optimization performance index,

The device parameter extraction method of the field-effect transistor characterized by making a device parameter when this optimization performance index shows an optimum state into an optimum solution.

[Claim 3]

In a device parameter extraction method according to claim 1 or 2,

A parasitic capacity by the circumference structure of said field-effect transistor, an inductance, the device parameter extraction method of a field-effect transistor with which resistance is also characterized by extracting to said device parameter and coincidence as an unknown.

[Claim 4]

In claims 1 and 2 or a device parameter extraction method given in 3,

Said fitting is the device parameter extraction method of the field-effect transistor characterized

by being carried out with the least square method.

[Translation done.]

* NOTICES *

JPO and NCIPi are not responsible for any damages caused by the use of this translation.

- 1.This document has been translated by computer. So the translation may not reflect the original precisely.
- 2.**** shows the word which can not be translated.
- 3.In the drawings, any words are not translated.

DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Field of the Invention]

This invention relates to the approach of extracting device parameters, such as capacity (Cgs) between the gate sources of a field-effect transistor, capacity (Cgd) between gate drains, and capacity (Cds) between the drain sources.

[0002]

[Description of the Prior Art]

The device parameter extract of a field-effect transistor was conventionally performed by s parameter of a transistor and fitting of a grounded source transistor small signal equivalent circuit by which the grounded source was carried out in many cases (nonpatent literature 1). Although many parameters are contained in a grounded source transistor small signal equivalent circuit Among those, capacity (Cgs) between the gate sources, capacity between gate drains (Cgd), Three kinds of capacity of the capacity (Cds) between the drain sources is most important parameters that determine the RF property of a transistor. Moreover, since it is not easy, it can be said to be the decision of the three above-mentioned kinds of capacity with the fitting activity using s parameter to extract these three kinds of capacity with a sufficient precision by approaches other than fitting which used s parameter.

[0003]

The sensibility to the optimization performance index of three kinds of capacity differs, respectively. In a grounded source, the capacity (Cgs) between the gate sources and the capacity (Cgd) between gate drains have the capacity (Cds) between the drain sources in the inclination for sensibility to be low, to having comparatively big sensibility. The value of the capacity (Cds) between the drain sources depends this on the relatively small thing, connecting with big drain conductance (gd) and juxtaposition, not working as a feedback capacity like the capacity (Cgd) between gate drains, etc. compared with other capacity. These things became a cause and the extract precision of the former of the capacity (Cds) between the drain sources was bad as compared with the capacity (Cgs) between the gate sources, or the capacity (Cgd) between gate drains.

[0004]

Moreover, the effect of not only the intrinsic part of a transistor but parasitic capacitance or a parasitism inductance is included in measured s parameter. The capacity (Cds) between the drain sources with the low sensibility to an optimization performance index will shift from a right value in response to the effect of a parasitism component easily. In order to improve this point, generally amending the effect of [other than an intrinsic device parameter] by actuation of s parameter beforehand is performed. The port extension method or the approach (nonpatent literature 2) of Aoki is this. However, the precision of a device parameter required of the ultrahigh frequency circuit design in a frequency domain 100GHz or more in recent years is

high, and since there is a limitation also in amendment of s parameter, the approach of the further amelioration is needed.

[0005]

That the bad influence of the sampling error of the capacity (C_d s) between the drain sources actualizes most is the case where a small signal equivalent circuit model is extrapolated and used for a high-frequency side from a fitting frequency range. the vector of today and s parameter -- a measurable frequency is to about 110GHz, and extrapolation of a small signal equivalent circuit model is needed in the frequency beyond this. On such frequencies, it had become the factor which a match condition and the estimated precision of a stability index fall [factor], and worsens the design nature of a circuit.

[0006]

[Nonpatent literature 1] Work besides Reza serious DIAHOI, a "100GHz high gain MMIC InP cascode amplifier" IEEE JANARUOBUS solid-state circuit, 1991, the 26th volume, 1370 - 1377 pages (1377 et al. Reza Majidi-Ahy and "100-GHzHigh-gain InP MMIC Cascode Amplifier" IEEE Journal of Solid-State Vol. 26, pp.1370- 1991)

[Nonpatent literature 2] the [the Aoki ****, a "S parameter measurement of package transistor" Institute of Electronics, Information and Communication Engineers paper magazine, C-II, 1990, and] -- a J73-C-II volume, No. 7, and 432 - 435 pages.

[0007]

[Problem(s) to be Solved by the Invention]

That the aforementioned problem occurs has a fundamental cause in using only fitting of a grounded source s parameter with the sensibility low about the capacity (C_d s) between the drain sources to an optimization performance index, and, as for the sensibility to an optimization performance index, the structure top of a field-effect transistor essentially is not improved, either.

[0008]

The purpose of this invention proposes the approach of highly precise s parameter fitting, and is to extract more the capacity (C_d s) between the drain sources whose extract precision whose sensibility to an optimization performance index was conventionally low, and was bad to high degree of accuracy.

[0009]

[Means for Solving the Problem]

Invention concerning claim 1 makes a port 1 the gate electrode of the field-effect transistor by which the grounded source was carried out, and measures a grounded source 2 port s parameter by making a drain electrode into a port 2. Although the grounded gate of this field-effect transistor was carried out, make a source electrode into a port 1 and a grounded gate 2 port s parameter is measured by making a drain electrode into a port 2. A grounded source transistor small signal equivalent circuit and a grounded gate transistor small signal equivalent circuit are constituted using a common device parameter. Fitting by said grounded source transistor small signal equivalent circuit to said grounded source 2 port s parameter, and fitting by said grounded gate transistor small signal equivalent circuit to said grounded gate 2 port s parameter It carried out to coincidence using one optimization performance index, and considered as the device parameter extraction method of the field-effect transistor characterized by making a device parameter when this optimization performance index shows an optimum state into an optimum solution.

[0010]

Invention concerning claim 2 is set to a device parameter extraction method according to claim 1. Make into a port 1 the gate electrode of the field-effect transistor by which the grounded drain was carried out, and a grounded drain 2 port s parameter is measured by making a source electrode into a port 2. A grounded drain transistor small signal equivalent circuit is

constituted using the aforementioned common device parameter. Three persons of fitting by said grounded drain transistor small signal equivalent circuit to said grounded drain 2 port s parameter and two persons' above mentioned fitting are performed to coincidence using one optimization performance index. It considered as the device parameter extraction method of the field-effect transistor characterized by making a device parameter when this optimization performance index shows an optimum state into an optimum solution.

[0011]

Invention concerning claim 3 also made a parasitic capacity by the circumference structure of said field-effect transistor, an inductance, and resistance the device parameter extraction method of the field-effect transistor characterized by extracting to said device parameter and coincidence as an unknown in the device parameter extraction method according to claim 1 or 2.

[0012]

Invention concerning claim 4 was taken as the device parameter extraction method of the field-effect transistor characterized by performing said fitting with the least square method in claims 1 and 2 or a device parameter extraction method given in 3.

[0013]

[Embodiment of the Invention]

s parameter measurement of RF TEG of the grounded source usually used in this invention (Test Element Group) -- in addition, s parameter of RF TEG of a grounded gate is measured, and fitting of the small signal equivalent circuit corresponding to coincidence is performed to both s parameter. Instead of being formed in fields other than the formation field of the semiconductor device in a semi-conductor wafer as a component for evaluation, and measuring the parameter of a semiconductor device directly, "TEG" measures the parameter of the component for evaluation, and gets to know the parameter of an actual semiconductor device indirectly. The device parameter extract by the grounded gate has high sensibility to an optimization performance index rather than a grounded source about the capacity (Cds) between the drain sources, while sensibility is lower than a grounded source about the capacity (Cgs) between the gate sources. For this reason, the extract precision of a device parameter can be improved by performing both fittings of a complementary grounded source and a grounded gate to coincidence.

[0014]

[The gestalt of the 1st operation]

RF TEG used for drawing 1 with the gestalt of operation of the 1st of this invention is shown. In drawing 1 (a) and (b), the electrode pad 2 is arranged so that s parameter measurement of two ports can be performed to the field-effect transistor 1 by which the grounded source was carried out, and the field-effect transistor 3 by which the grounded gate was carried out. Moreover, drawing 1 (c) is transmission-line RF TEG with which the part of the transistors 1 and 3 of drawing 1 (a) and (b) was replaced to the straight-line-like transmission line 5.

[0015]

First, a 2 port s parameter is measured about RF TEG of drawing 1 (c), and the circuit constant contained in the equal circuit 7 (refer to drawing 2) of the electrode pad 2 for measurement is determined. About the transmission line 5 of the shape of a straight line of drawing 1 (c), analysis is easily possible for the property theoretically. Then, s parameter of the transmission line 5 of the shape of said straight line is calculated analytically, the equal circuit 7 showing the electrode pad 2 for measurement of RF TEG of drawing 1 (c) can be assumed, and the equivalent circuit parameter of the electrode pad 2 for measurement can be determined by performing fitting to the 2 port s parameter measured about drawing 1 (c). However, the effect of the electrode pad 2 for measurement is small, and when the contribution to the 2 port s parameter of the grounded source field-effect transistor 1 or the 2 port s parameter of the

grounded gate field-effect transistor 3 can be disregarded, it is not necessary to do the above-mentioned activity.

[0016]

Next, fitting of the grounded source transistor small signal equivalent circuit of the 2 port s parameter measured about RF TEG of drawing 1 (a) and (b), drawing 2 (a), and (b) and a grounded gate transistor small signal equivalent circuit is performed. This grounded source transistor small signal equivalent circuit and a grounded gate transistor small signal equivalent circuit are constituted using the common device parameter. In drawing 2 the equal circuit of the electrode pad 2 for measurement and 8 7 The equal circuit of the transmission line 4, The capacity (Cgs) between the gate sources and 10 9 The capacity between gate drains (Cgd), The capacity (Cds) between the drain sources and 12 11 A source inductance, The current source as which 13 expresses gate resistance and the resistance to which in source resistance and 15 Ra and 17 express Rb and, as for 18, drain resistance and 16 express [14] drain conductance, and 19 expresses a drain current, and 20 are gate inductances. It is $gm = gm_0 \exp(-j\omega\tau)$. gm is [the mutual conductance in DC and tau of a mutual conductance and gm0] the electronic channel transit times.

[0017]

Since the equivalent circuit parameter of an equal circuit 7 which expresses the electrode pad 2 for measurement which carried out electrical parameter extraction from RF TEG of drawing 1 (c) in the case of this example is known, it is fixed to the value. However, when the effect of the electrode pad 2 for measurement can disregard the contribution to the 2 port s parameter of the grounded source field-effect transistor 1, or the 2 port s parameter of the grounded gate field-effect transistor 3 small, even if it deletes the equal circuit 7 showing the electrode pad 2 for measurement, it does not interfere.

[0018]

Moreover, about the short transmission line 4 which exists between the electrode pad 2 for measurement shown in drawing 1, and a transistor, as shown in drawing 2, the value is determined as fitting and coincidence of the intrinsic parameters 9-20 of a transistor supposing the equal circuit 8 by capacity and the inductor. However, the effect of said transmission line 4 is small, and when the contribution to the 2 port s parameter of the grounded source field-effect transistor 1 or the 2 port s parameter of the grounded gate field-effect transistor 3 can be disregarded, even if it deletes the equal circuit 8 showing said transmission line 4, it does not interfere.

[0019]

Moreover, the gate inductance 20 which generates parasitically the source inductance 12 parasitically generated to the transistor 1 by which the grounded source was carried out to the transistor 3 by which the grounded gate was carried out is made into the parameter. However, the effect of these source inductance 12 or the gate inductance 20 is small, and when the contribution to the 2 port s parameter of the grounded source field-effect transistor 1 or the 2 port s parameter of the grounded gate field-effect transistor 3 can be disregarded, even if it deletes the equal circuit showing said source inductance 12 and gate inductance 20, it does not interfere.

[0020]

Moreover, the gate resistance 13 which can be extracted by approaches other than fitting with s parameter among the intrinsic parameters 9-20, source resistance 14, and drain resistance 15 grade are extracting beforehand, and can be improved in fitting precision with s parameter.

[0021]

One optimization performance index estimates the fitting error over the 2 port s parameter of the grounded source field-effect transistor 1 obtained from the high frequency TEG of drawing 1 (a), and the fitting error over the 2 port s parameter of the grounded gate field-effect

transistor 3 obtained from the high frequency TEG of drawing 1 (b). Moreover, it may carry out by doubling fitting of the grounded drain transistor small signal equivalent circuit of the 2 port s parameter measured about grounded drain RF TEG of drawing 1 (d), and drawing 2 (c), and one optimization performance index may estimate three kinds of fitting errors, a grounded source, a grounded gate, and a grounded drain.

[0022]

It is possible to use what added the absolute value of the difference of s parameter about the group of all s parameters, for example, and the thing which involves the absolute value of said difference and was added about the group of all s parameters as an optimization performance index. Moreover, weight may be attached to specific s parameter.

[0023]

It is the following formula when an example showing the optimization performance index Cost by the least square method to which weight was attached is shown.

$$Cost = W_s \sum_{i=1}^2 \sum_{j=1}^2 \sum_{f=1}^m \left[\frac{(S^* smij - S smij)}{S^* smij} \right]^2 + W_g \sum_{i=1}^2 \sum_{j=1}^2 \sum_{f=1}^m \left[\frac{(S^* gmij - S gmij)}{S^* gmij} \right]^2 \quad (1)$$

** -- it becomes like. Here, S expresses s parameter of a small signal equivalent circuit, and the 2 port s parameter with which S* was measured, further, in a grounded source and g, a grounded gate and m express a test frequency (specific frequency of the 1st to the m-th inside currently prepared beforehand), and i and j express [s of a suffix] the port (1 2) of s parameter. Ws and Wg are the weight to the fitting error of a grounded source and a grounded gate, respectively.

[0024]

In a formula (1), the 1st term of the right-hand side expresses the fitting error of a grounded source, the 2nd term expresses the fitting error of a grounded gate, and both are added. That is, by this formula (1), a small signal equivalent circuit parameter will be determined that the sum total of the fitting error of a grounded source and a grounded gate will become min.

[0025]

In addition, various things as an optimization performance index can be used. For example, s parameter may be divided into real part and imaginary part, the difference of an actual measurement and calculated value may be calculated respectively, and the absolute value may be added and united. Moreover, s parameter is displayed in a polar-coordinate format, difference with calculated value is calculated by dividing into an absolute value and an include angle, and even if it adds and unites the absolute value, it can use as an optimization performance index. Essentially, the improvement effect of this invention does not receive effect in the mathematical expression of an optimization performance index.

[0026]

Drawing 3 (a), (b), and (c) express the sensibility to the optimization performance index of the capacity (Cgs) 9 between the gate sources which is an intrinsic parameter, the capacity (Cgd) 10 between gate drains, and the capacity (Cds) 11 between the drain sources. Usually, when using grounded source RF TEG used (x mark), while the sensibility to the capacity (Cgs) 9 between the gate sources is high, the sensibility to the capacity (Cds) 11 between the drain sources is low. Moreover, when using grounded gate RF TEG (** mark), while the sensibility to the capacity (Cds) 11 between the drain sources is high, the sensibility to the capacity (Cgs) 9 between the gate sources is low. The approach (thick wire) by this invention is understood that sensibility is high with sufficient balance to all parameters (Cgs, Cgd, Cds) to these. This effectiveness can perform [the extract of the intrinsic device parameters 9-20] now in a higher

precision.

[0027]

[Effect of the Invention]

It is size according to this invention, for the electrical-parameter-extraction precision of a field-effect transistor to be improved, and to become possible to extract more the capacity (Cds) between the drain sources whose extract precision whose sensibility to an optimization performance index was low, and was bad to high degree of accuracy, as explained above, and to ** to improvement in the design nature in a circuit design.

[Brief Description of the Drawings]

[Drawing 1] (a), (b), (c), and (d) are the explanatory views of RF TEG of a grounded source, a grounded gate, the transmission line, and a grounded drain.

[Drawing 2] (a), (b), and (c) are the circuit diagrams of the small signal equivalent circuit of a grounded source, a grounded gate, and a grounded drain.

[Drawing 3] (a), (b), and (c) are the property Figs. showing the sensibility to the optimization performance index of the capacity (Cgs) between the gate sources which is an intrinsic parameter, the capacity (Cgd) between gate drains, and the capacity (Cds) between the drain sources.

[Description of Notations]

- 1: Grounded source transistor
- 2: The electrode pad for measurement
- 3: Grounded gate transistor
- 4: Transmission line
- 5: Straight-line-like transmission line
- 6: Grounded drain transistor
- 7: The equal circuit of the electrode pad for measurement
- 8: The equal circuit of a transmission-line part
- 9: Capacity between the gate sources (Cgs)
- 10: Capacity between gate drains (Cgd)
- 11: Capacity between the drain sources (Cds)
- 12: Source inductance
- 13: Gate resistance
- 14: Source resistance
- 15: Drain resistance
- 16:Ra
- 17:Rb
- 18: Resistance showing drain conductance
- 19: The current source showing a drain current
- 20: Gate inductance

[Translation done.]

* NOTICES *

JPO and NCIPi are not responsible for any damages caused by the use of this translation.

- 1.This document has been translated by computer. So the translation may not reflect the original precisely.
- 2.**** shows the word which can not be translated.
- 3.In the drawings, any words are not translated.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1] (a), (b), (c), and (d) are the explanatory views of RF TEG of a grounded source, a grounded gate, the transmission line, and a grounded drain.

[Drawing 2] (a), (b), and (c) are the circuit diagrams of the small signal equivalent circuit of a grounded source, a grounded gate, and a grounded drain.

[Drawing 3] (a), (b), and (c) are the property Figs. showing the sensibility to the optimization performance index of the capacity (C_{gs}) between the gate sources which is an intrinsic parameter, the capacity (C_{gd}) between gate drains, and the capacity (C_{ds}) between the drain sources.

[Description of Notations]

- 1: Grounded source transistor
- 2: The electrode pad for measurement
- 3: Grounded gate transistor
- 4: Transmission line
- 5: Straight-line-like transmission line
- 6: Grounded drain transistor
- 7: The equal circuit of the electrode pad for measurement
- 8: The equal circuit of a transmission-line part
- 9: Capacity between the gate sources (C_{gs})
- 10: Capacity between gate drains (C_{gd})
- 11: Capacity between the drain sources (C_{ds})
- 12: Source inductance
- 13: Gate resistance
- 14: Source resistance
- 15: Drain resistance
- 16: R_a
- 17: R_b
- 18: Resistance showing drain conductance
- 19: The current source showing a drain current
- 20: Gate inductance

[Translation done.]

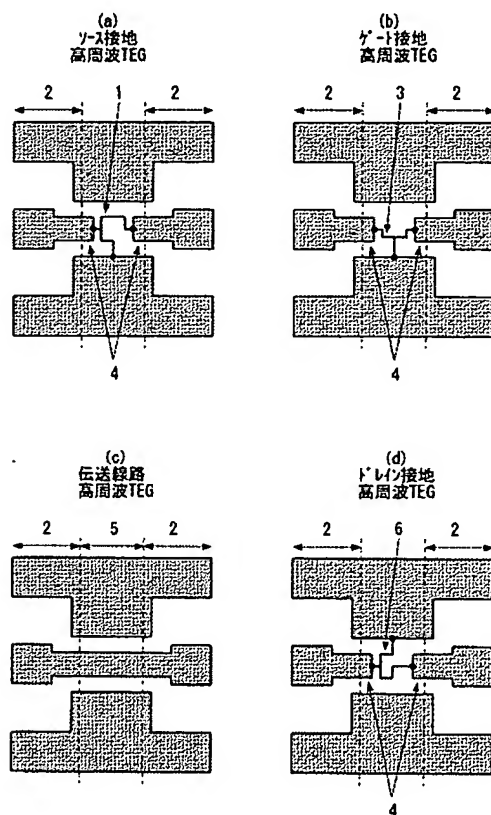
* NOTICES *

JPO and NCIPi are not responsible for any damages caused by the use of this translation.

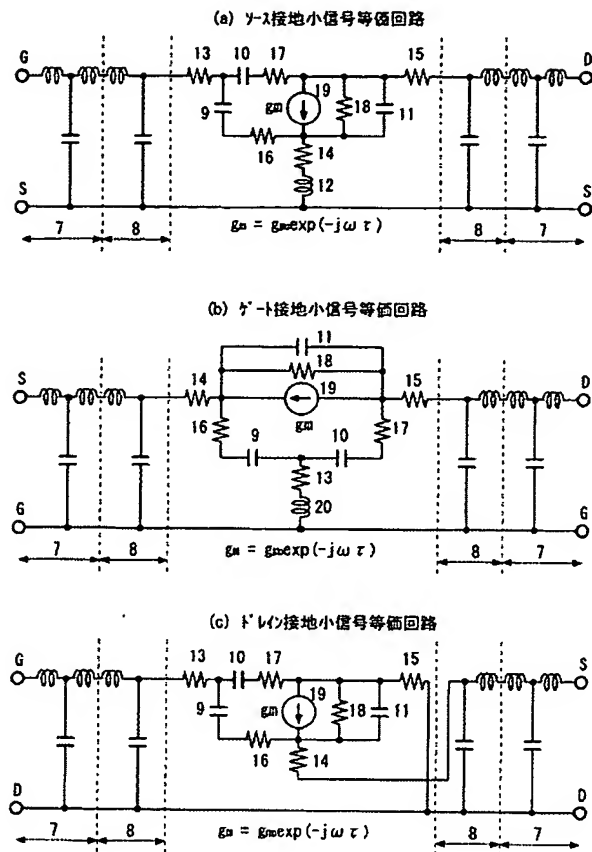
- 1.This document has been translated by computer. So the translation may not reflect the original precisely.
- 2.**** shows the word which can not be translated.
- 3.In the drawings, any words are not translated.

DRAWINGS

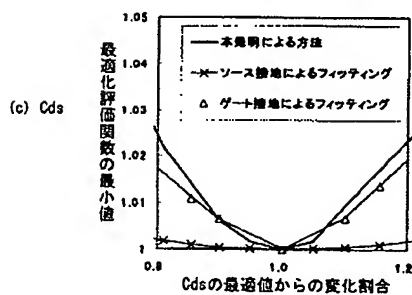
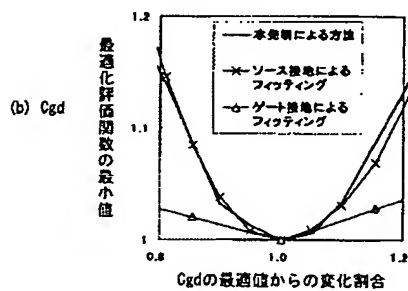
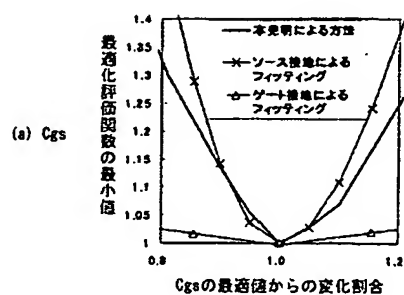
[Drawing 1]



[Drawing 2]



[Drawing 3]



[Translation done.]